

HSMP-3866

Quad PIN Diode Pi Attenuator 300 kHz to 3 GHz
in SOT 25 Package

AVAGO
TECHNOLOGIES

Data Sheet



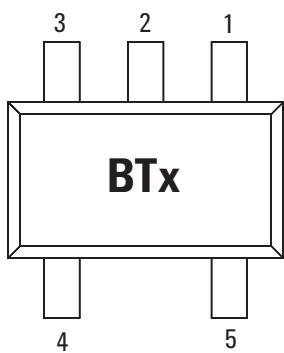
Description

Avago Technology's HSMP-3866 is a wideband, low insertion loss, low current, Quad PIN Diode Pi Attenuator in a low cost surface mount SOT-25 package. It provides a good match and flat attenuation over an extremely wide band from 300 kHz to 3 GHz.

The SOT-25 packages gives a reduction in part count and takes up less space on board compared to multi package solutions.

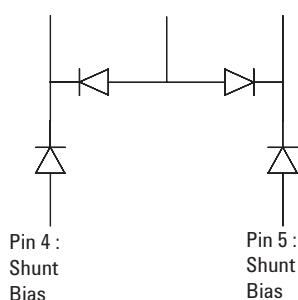
Four PIN Diodes in one package encourages performance repeatability for improved production yield at board level.

Package Marking and Pin connections



Note:
Package marking provides orientation and identification
"BT"= Device Code
"x" = Month code indicates the month of manufacture

Pin 3 : Pin 2 : Pin 1 :
RF In/Out Series Bias RF In/Out



Features

- 4 PIN Diodes in a SOT-25 package
- 300 kHz to 3 GHz usable frequency band
- Low Current
- Low insertion Loss
- MSL-1 and Lead-free
- Tape & Reel packaging option available

Specification At 1 GHz, V+=1.2V

- IIP3 = 30 dBm (Typical)
- Attenuation = 36 dB (Typical)
- Insertion Loss = -2.5 dB (Typical)
- Return Loss = -18 dB (Typical)

Application

- Broadband system application (i.e., CATV, WCDMA, etc)
- General purpose Voltage-Control-Attenuator for low current applications.

Absolute Max Ratings [1], $T_c = +25^\circ\text{C}$

Symbol	Parameter	Unit	Abs Max
I_f	Forward Current (1 μs Pulse)	Amp	1
P_{IV}	Peak Inverse Voltage	V	50
T_j	Junction Temperature	$^\circ\text{C}$	150
T_{stg}	Storage Temperature	$^\circ\text{C}$	-65 to 150
θ_{jb}	Thermal Resistance ^[2]	$^\circ\text{C}/\text{W}$	167

Notes :

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. Thermal Resistance is measured from junction to board using IR method.

Electrical Specifications, $T_c = +25^\circ\text{C}$ (Each Diode)

	Minimum Breakdown Voltage V_{BR} (V)	Typical Series Resistance R_s (Ω)	Typical Total Capacitance C_T (pF)
	50	3.0/1.5*	0.22
Test Condition	$V_R = V_{BR}$ Measure $I_R \leq 10 \mu\text{A}$	$I_F = 10 \text{ mA}, f = 100 \text{ MHz}$ $I_F = 100 \text{ mA}^*$	$V_R = 50 \text{ V}$ $f = 1 \text{ MHz}$

Typical Performance, $T_c = +25^\circ\text{C}$ (Each Diode)

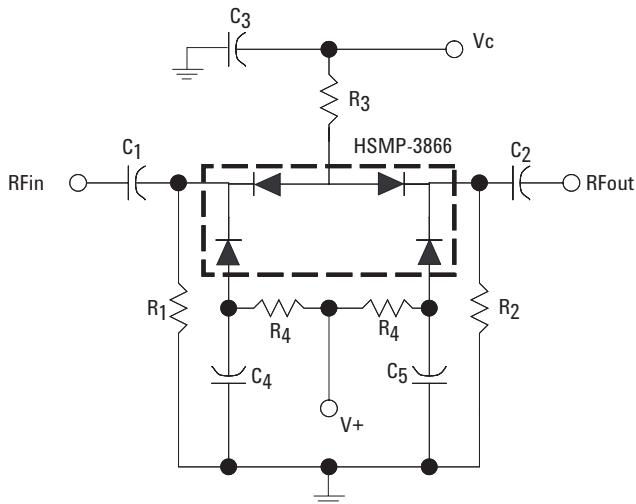
	Total Resistance R_T (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
	22	500	80	0.22
Test Condition	$I_F = 1 \text{ mA}$ $f = 1 \text{ MHz}$	$I_F = 10 \text{ mA}$ $I_R = 250 \text{ mA}$	$V_R = 50 \text{ V}$ $I_F = 10 \text{ mA}$ 90% Recovery	$V_R = 50 \text{ V}$ $f = 1 \text{ MHz}$

Typical Performance for HSMP-3866 Quad PIN Diode π Attenuator @ $+25^\circ\text{C}$

Parameter	Test Condition	Units	Typical
Insertion Loss	$V_c = 5\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 1 \text{ GHz}$	dB	-2.5
Return Loss	$V_c = 0\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 1 \text{ GHz}$	dB	-18
Attenuation	$V_c = 0\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 1 \text{ GHz}$	dB	36
IP3	$V_c = 1.5\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 1 \text{ GHz}$	dBm	30
IP3	$V_c = 5.0\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 1 \text{ GHz}$	dBm	40
IP3	$V_c = 1.5\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 300 \text{ MHz}$	dBm	25
IP3	$V_c = 5.0\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 300 \text{ MHz}$	dBm	37
IP3	$V_c = 1.5\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 100 \text{ MHz}$	dBm	23
IP3	$V_c = 5.0\text{V}, V_+ = 1.2\text{V}, \text{Freq} = 100 \text{ MHz}$	dBm	35

Notes :

1. Measurement above obtained using Wideband RF circuit design shown in Figure 1 & 2



Component	Value
R1, R2	620 Ω
R3	390 Ω
R4	2200 Ω
C1 - C5	10 nF

Figure 1. Wideband Quad PIN Diode π Attenuator Circuit

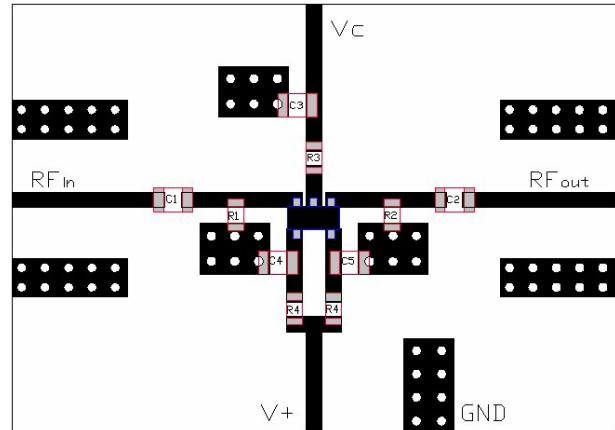


Figure 2. Circuit Board Layout.

Typical Performance Curves for Single Diode @ $T_c = +25^\circ\text{C}$

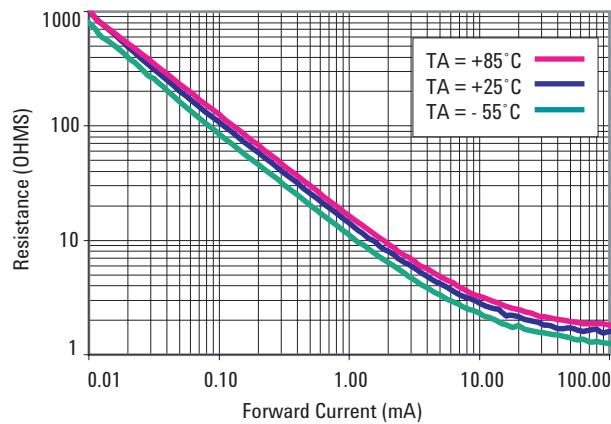


Figure 3. RF Resistance vs. Forward Bias Current

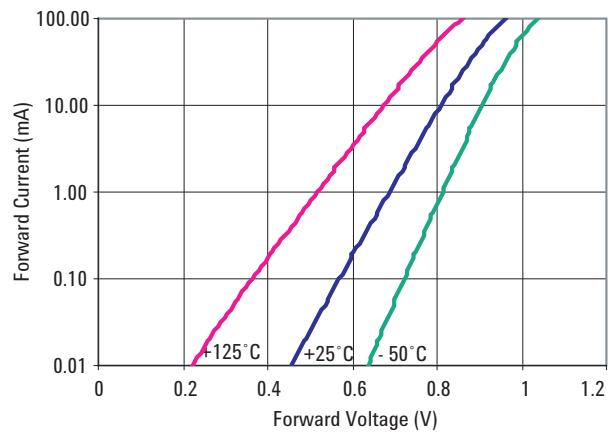


Figure 4. Forward Current vs. Forward Voltage

Typical Performance Curves for Single Diode @ $T_c = +25^\circ C$

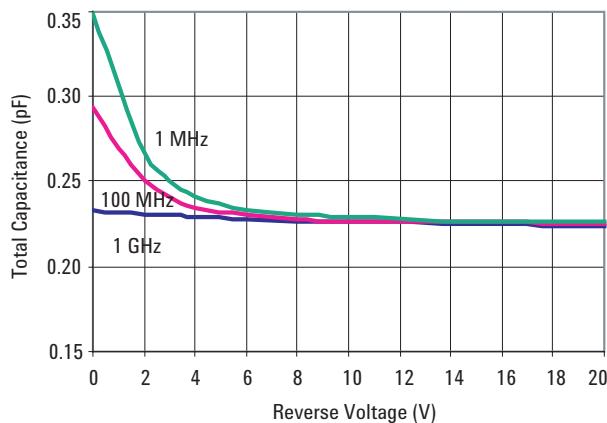


Figure 5. RF Capacitance vs Reverse Bias

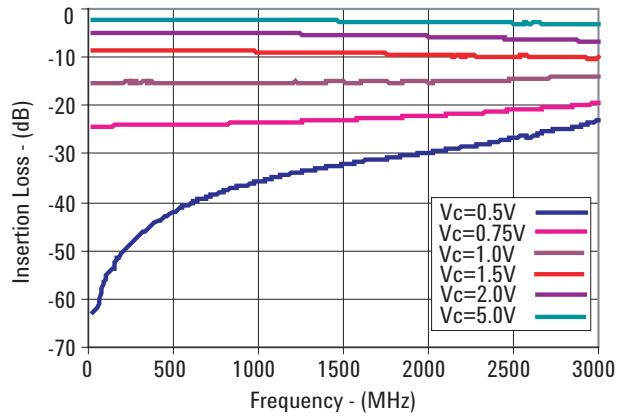


Figure 6. Insertion Loss vs. Frequency

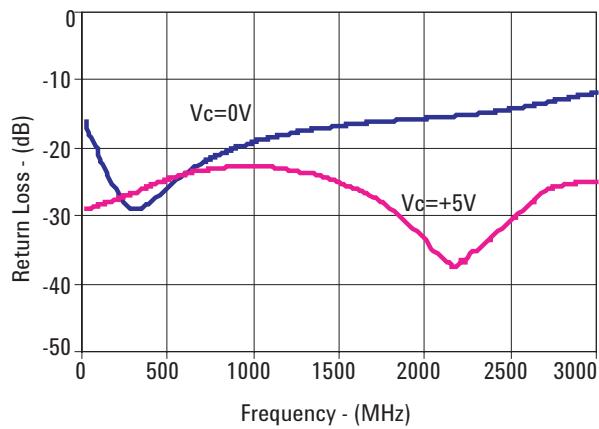


Figure 7. Return Loss vs. Frequency

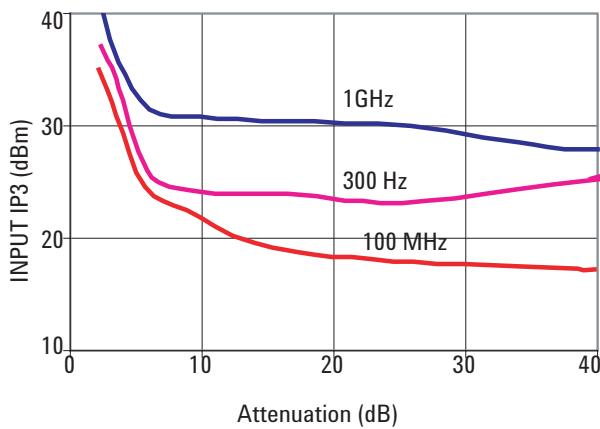


Figure 8. Input IP3 vs. Attenuation

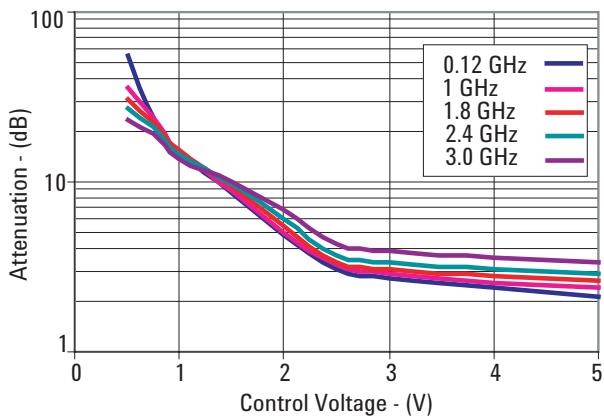
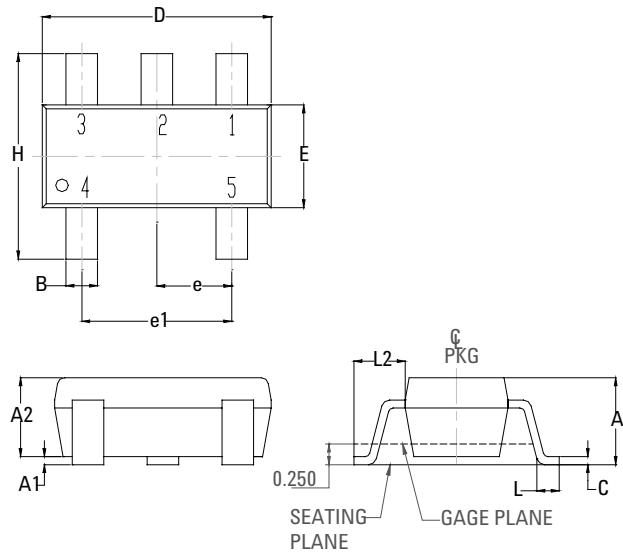


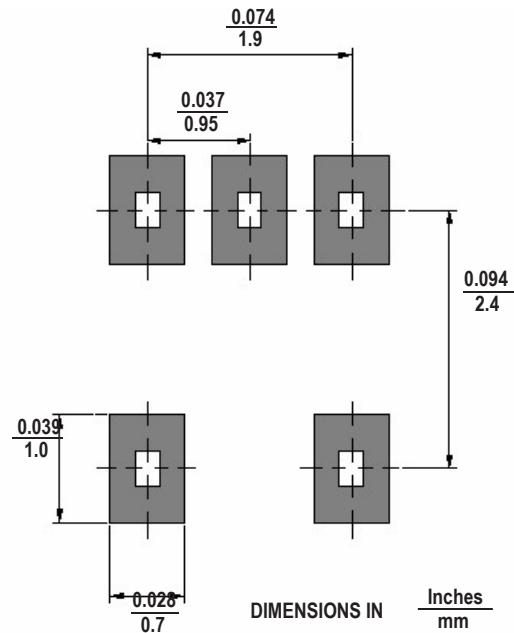
Figure 9. Attenuation vs. Control Voltage

Package Outline & Dimension

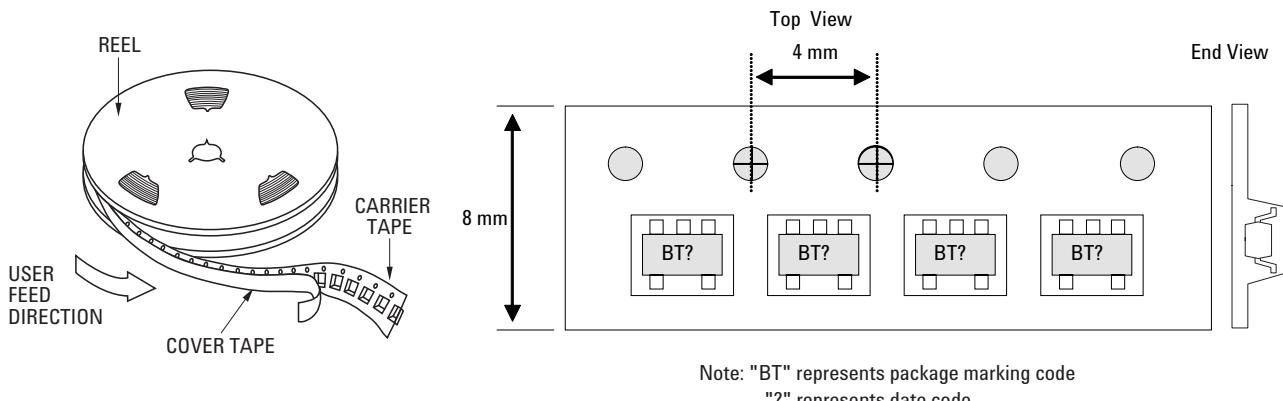


Symbol	Dimension		
	Minimum	Nominal	Maximum
D	2.80	2.90	3.00
H	2.60	2.80	3.00
E	1.50	1.60	1.70
e1	1.88	1.90	1.92
e	0.93	0.95	0.97
B	0.35		0.50
A2	0.9	1.15	1.30
C	0.08		0.22
L	0.35		0.60
A1	0		0.15
A	0.9		1.40

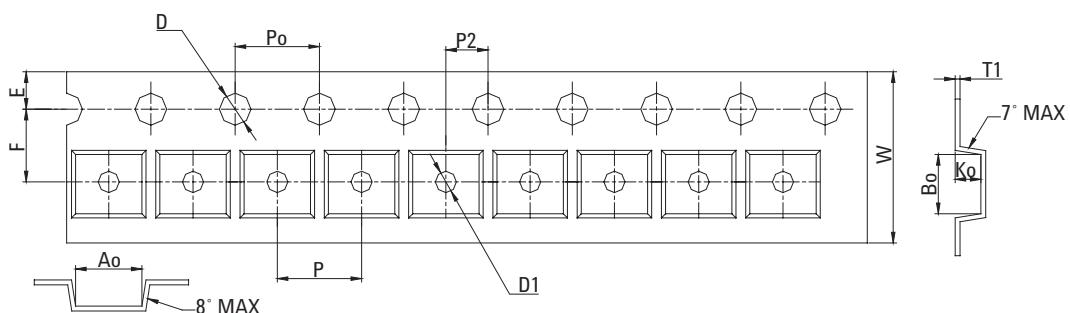
PCB Footprint



Device Orientation



Tape Dimension



Symbol	Milmeters		
	Nominal	Minimum	Maximum
V	8.00 (0.315)	7.90 (0.311)	8.30 (0.327)
P	4.00 (0.157)	3.90 (0.154)	4.10 (0.161)
E	1.75 (0.069)	1.65 (0.065)	1.85 (0.073)
F	3.50 (0.138)	3.45 (0.136)	3.55 (0.140)
J	1.50 (0.059)	N/A	1.60 (0.063)
J1	1.00 (0.039)	N/A	1.25 (0.049)
Po	4.00 (0.157)	3.90 (0.154)	4.10 (0.161)
P2	2.00 (0.079)	1.95 (0.077)	2.05 (0.081)
Ao	3.23 (0.127)	3.13 (0.123)	3.33 (0.131)
Jo	3.81 (0.125)	3.08 (0.121)	3.28 (0.129)
Fo	1.60(0.063)	1.50 (0.059)	1.70 (0.067)
T1	0.254 (0.0100)	0.241 (0.0095)	0.267 (0.0105)

Part Number Ordering Information

Part number	No of Device	Container
HSMP-3866-BLKG	100	Anti-static bag
HSMP-3866-TR1G	3000	7" reel
HSMP-3866-TR2G	10000	13" reel

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries. Data subject to change. Copyright © 2005-2009 Avago Technologies. All rights reserved. Obsolete 5989-4497EN
AV02-1962EN - June 3, 2009

AVAGO
TECHNOLOGIES